GoWin Development kit

Part number	Device Family	Device	Description
DK_START_GW1NSR-LV4CQN48GC7I6_V1.1	GW1NSR	GW1NSR4	The development board adopts the GW1NSR4 chip, the first generation products in the LittleBee® family. It is one form of SIP chip that integrates the GW1NS chip and PSRAM memory. It supports an ARM Cortex-M3 hard core processor, USB2.0 PHY, user flash, and ADC convertor.
DK_USB2.0_GW2AR-LV18QN88PC7I6_GW1NSR_LV4MG64PC7I6_V1.0	USB2.0	USB2.0	DK_USB2.0_GW2AR-LV18QN88PC7I6_GW1NSR-LV4MG64PC7I6_ V1.0 development board can apply to USB communication test, including USB 2.0 and USB 1.1 communication; the function evaluation of GW1NSR-4 and GW2AR-18 series of FPGA; hardware reliability verification; and software learning and debugging
DK_START_GW1N-LV4LQ144C6I5_V1.1	GW1N	GW1N-4	DK_START_GW1N-LV4LQ144C6I5_V1.1 development board adopts GOWIN LittleBeeTM FPGA family products, with features of low-power, instant start-up, high security, low cost, easy extension, which can effectively reduce the learning cost and help users quickly access to the design and development of programmable logic devices.
DK_START_GW1N-LV9LQ144C6I5_V2.1	GW1N	GW1N-9	DK_START_GW1N-LV9LQ144C6I5_V2.1 development board adopts GOWIN LittleBeeTM FPGA family products, with features of low-power, instant start-up, high security, low cost, easy extension, which can effectively reduce the learning cost and help users quickly access to the design and development of programmable logic devices.
DK_START_GW1N-LV9EQ144C6I5_V2.1	GWN	GW1N-9	The development board uses Gowin GW1N-9 FPGA devices. The GW1N series of FPGA products are the first generation of the Gowin LittleBee® family and it is an SIP chip. It has the characteristics of low power consumption, instant-start, low cost, non-volatility, high security, rich packages, convenient and flexible usage, etc., which can effectively reduce the learning cost and help users quickly enter the design and development field of programmable logic devices.
DK_START_GW1NR-LV9LQ144PC6I5_V3.1	GW1NR	GW1NR-9	The development board adopts the GW1NR-9 device, which is embedded with PSRAM of 64Mbit, user flash memory and other resources.
DK_START_GW2A-LV18PG256C8I7_V2.0	GW2A	GW2A18	The GOWIN DK_START_GW2A-LV18PG256C8I7_V2.0 Development Kit includes a DDR3 chip with 2Gbit storage space, 16-bit data bus width, and high data speed of 1600MT/s. The two Gigabit Ethernet interfaces support 10M, 100M, and 1000M Ethernet communication. The Board offers a wide array of peripheral interfaces, including LVDS, an SD card slot, and GPIO.
DK_START_GW2A-LV55PG484C8I7_V1.3	GW2A55	GW2A	DK_START_GW2A-LV55PG484C8I7_V1.3 development board includes a DDR3 chip with 2Gbit, 16-bit bus width. Its two Gigabit Ethernet interfaces support 10M, 100M, 1000M Ethernet communication. It has abundant peripheral interfaces, including LVDS interfaces, a SD card socket, CAN bus interface, MIPI CSI, MIPI DSI, AD/DA interface and GPIO interfaces. RTC module is designed to provide real-time clock for MCU IP. Besides that, it also offers an external Flash, switches, keys, LED, etc.
DK_START_GW2AR-LV18EQ144PC8I7_V1.1	GW2AR	GW2AR18	DK_START_GW2AR-LV18EQ144PC8I7_V1.1 Development Kit is a platform for evaluating the performance of the GW2AR-18 FPGAs. The Arora® GW2AR FPGAs offer an embedded 64Mbit PSRAM and a streamlined FPGA architecture with a 55nm process. These features make the GW2AR suitable for high-speed and low-cost applications. The DK_START_GW2AR-LV18EQ144PC8I7_V1.1 Development Kit offers rich external interfaces, including LVDS, GPIO, slide switches, key switches, LEDs, reset, and clock resources. The DK_START_GW2AR-LV18EQ144PC8I7_V1.1 Board provides a USB download interface. The data stream file can be downloaded to the internal SRAM or the external flash as needed.
DK_START_GW1NZ-LV1FN32C6I5_V3.1	GW1NZ	GW1NZ1	DK_START_GW1NZ-LV1FN32C6I5_V3.1 uses the GW1NZ-1 device. The GW1NZ series of FPGA products are the first generation of the LittleBee® family. They offer low power consumption, instant on, low cost, non-volatile, high security, various packages, and flexibility. They can be widely used in communication, industry control, consumer, video control, etc.
DK-START-GW1NS2 V2.1	GW1NS	GW1NS2	The DK-START-GW1NS2 V2.1 development board uses GOWIN's GW1NS-2C SoC FPGA device. The SoC FPGA embeds an ARM Cortex-M3 hard processor with a 2K LUT FPGA fabric. In addition, the GW1NS family of FPGA products includes a USB 2.0 PHY, user flash, and an 8 channel ADC. With the ARM Cortex-M3 hard processor as the core, the minimum memory required to implement system functions is included. The embedded FPGA logic module is convenient and flexible and can implement a variety of peripheral control functions, providing excellent computing capability. System response interrupt, high performance, low power consumption, flexible use, instant start, low cost, non-volatile memory, high security, easy to expand, etc., can effectively reduce learning costs, helping users to quickly enter programmable logic device design and development areas.
DK_START_GW1NS-LV4CQN48C7I6_V1.1	GW1NS	GW1NS4	The development board adopts the GW1NS-4 SoC FPGA. SoC FPFA is embedded with an ARM Cortex-M3 hard core processor. When the ARM Cortex-M3 hard-core processor is employed as the core, the needs of the Min. memory can be met. This board also supports USB2.0 PHY, user flash, and ADC convertor. The FPGA logic resources and other embedded resources can flexibly facilitate the peripheral control functions, which provide excellent calculation functions and exceptional system response interrupts. They also offer high performance, low power consumption, flexible usage, instant start-up, affordability, nonvolatile, high security, and abundant package types, among other benefits. It can be widely used in industrial control, communication, Internet of things, servo drive, consumer, and other industries.
DK_START_GW1NSR-LX2CQN48PC5I4_V2.1	GW1NSR	GW1NSR2	The development board adopts the GW1NSR-2 SoC FPGA. SoC FPFA is embedded with an ARM Cortex-M3 hard core processor, 32Mbit PSRAM, 1Mbit User Flash and eight-channel ADC converter, etc. When the ARM Cortex-M3 hard-core processor is employed as the core, the needs of the Min. memory can be met. FPGA logic resources and other embedded resources can flexibly facilitate the peripheral control functions, which provide excellent calculation functions and exceptional system response interrupts. They also offer high performance, low power consumption, flexible usage, instant start-up, affordability, nonvolatile, high security, and abundant package types, among other benefits.
DK_START_GW1NSR-LV4CQN48PC7I6_V1.1	GWNSR	GW1NSR4	The development board adopts the GW1NSR4 chip, the first generation products in the LittleBee® family. It is one form of SIP chip that integrates the GW1NS chip and PSRAM memory. It supports an ARM Cortex-M3 hard core processor, USB2.0 PHY, user flash, and ADC convertor.
DK_GoAI_GW2AR-LV18QN88PC8I7_V1.1	GW2AR-18	GW2AR	The development board uses Gowin GW2AR-18 FPGA devices embedded with 64 Mbit PSRAM. The GW2AR series of FPGA products are the first generation products of Gowin Arora family. As a kind of SIP chips, the GW2AR series of FPGA products offer a range of features and rich resources like high-performance DSP, high-speed LVDS interface and BSRAM. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2A series of FPGA products ideal for high-speed and low-cost applications.
DK_GoAI_GW1NSR-LV4CQN48PC7I6_V2.2	GW1NSR	GW1NSR	The development board adopts the GW1NSR-4 SoC FPGA. SoC FPFA is embedded with an ARM Cortex-M3 hard core processor. When the ARM Cortex-M3 hard-core processor is employed as the core, the needs of the Min. memory can be met. FPGA logic resources and other embedded resources can flexibly facilitate the peripheral control functions, which provide excellent calculation functions and exceptional system response interrupts. They also offer high performance, low power consumption, flexible usage, instant start-up, affordability, nonvolatile, high security, and abundant package types, among other benefits. The development board offers HDMI interface, and FPC interface of camera. There are also button, LED and other resources for developers or fans to learn to use.
DK_VIDEO_GW2A-LV18PG484C8I7_V1.2	GW2A	GW2A18	DK_VIDEO_GW2A-LV18PG484C8I7_V1.2 applies to high-speed data storage based on DDR3, high-speed communication test based on LVDS and HDMI RX/TX, 18k series of FPGA evaluation, the hardware verification and software learning and debugging, etc. The development board uses the GW2A- LV18PG484 FPGA device, which is the first generation of Gowin Arora family. The GW2A series of FPGA products offer a range of features and rich resources like high-performance DSP, high-speed LVDS interface and BSRAM. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2A series of FPGA products ideal for high-speed and low-cost applications. The development board includes a DDR3 chip with 2Gbit storage space and 16 bits data bus width. It integrates four HDMI interfaces, two of which are used to receive signals (One receives signals via decoding chip, and the other receives signals via FPGA IP), and the other two are used to transmit signals (One transmits signals via decoding chip, and the other transmits signals via FPGA IP). Besides that, this board also includes abundant external interfaces, including LVDS TX, LVDS RX, MIPI CSI, MIPI DSI, and GPIO. The external Flash is used to store FPGA configuration programs. Slide switches, keys, and LED facilitate users debugging.
GOWIN FPGA DOWNLOAD CABLE	GW1N/NR, GW2A/AR		Gowin FPGA Download Cable is used to connect USB to JTAG Ports for downloading FPGA Bit-File from host PC to program GW FPGA devices on PCB Board.
4 JTAG interface offline programmer			Gowin USB download cable is mainly used to download the bit stream file generated by Gowin Yunyuan software to Gowin FPGA chip or external storage device.
16 JTAG interface offline programmer			Offline programmer is a device that offline programs GW1N(R) chips. It has the features of data confidentiality, portability, multi-path programming, etc. It is suitable for rapidly large-volume production at the factory and is convenient for maintenance personnel to carry out. The offline programmer can simultaneously program sixteen FPGA devices, which greatly increases the mass production rate. The offline programmer encrypts and saves the data using an AES-128 advanced encryption algorithm, and the key is saved after several times of encrypting. AES is a set of internationally recognized, commonly used and secure encryption standards that ensure securely delivering data.